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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,428	08/05/2003	Taku Ishizawa	405507/0012	8311

7590 07/07/2005

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EXAMINER	
NGUYEN, LAM S	

ART UNIT	PAPER NUMBER
2853	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

GM

Office Action Summary	Application No.	Applicant(s)	
	10/634,428	ISHIZAWA ET AL.	
	Examiner	Art Unit	
	LAM S. NGUYEN	2853	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 5 is objected to because of the claim includes "a power supply terminal" that has been cited in claim 1. Appropriate correction is required.

Claim 10 is objected to because of the claim includes "a control signal terminal" and "a power supply terminal" that have been cited in claim 8. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-5 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murray et al. (US 5610635) in view of Nagata et al. (US 5838549).

Referring to claims 1, 8:

Murray et al. discloses a circuit board (*FIG. 6*) having a storage device (*FIG. 6, element 49*) for storing data relating to a marking material for printing cartridge having a substantially rectangular shape, said circuit board comprising:

at least two ground terminals (*FIG. 6, elements 1 and 9*) arranged on said circuit board at two edges thereof that are located on one axis thereof; and

a plurality of terminals (*FIG. 6, elements 1-10*) arranged on said

circuit board, for read/write operations on said data relating to the marking material for printing, said plurality of terminals including a power supply terminal (*FIG. 6, elements 2, 8, 10*) and a control signal terminal (*FIG. 6, elements 3-7*).

Murray et al. does not disclose wherein said at least two ground terminals are not the terminals in closest proximity to said power supply terminal.

Nagata et al. disclose a circuit board having a storage device (*FIG. 1, element 3*) and plurality of terminals (*FIG. 1, element 41*) for electrical connecting to the storage device to other components. The terminals include at least a ground terminal (*FIG. 1, element Gnd*) arranged at an edge of the board and a power supply terminal (*FIG. 1, element Vcc*), wherein the ground terminal is not the terminals in closest proximity to the power supply terminal.

Therefore, it would have been obvious for one having ordinary skill in the art at the time invention was made to modify the circuit board disclosed by Murray et al. to locate the power supply terminal not being proximity to the ground terminals as disclosed by Nagato et al. because this is a common technique well known in the art to avoid the risk of short circuit due to current licking between the closed terminals or dust located between the terminals.

Murray et al. also disclose the following claimed invention:

Referring to claim 2: wherein said plurality of terminals and said ground terminals are arranged in a single row with two of said at least two ground terminals being located at the outermost ends of said row (*FIG. 6: The row includes terminals 1, 3, 5, 7, and 9*).

Referring to claims 3, 9: wherein said plurality of terminals are arranged to form a plurality of rows parallel to one side of said circuit board (*FIG. 6: The terminals are arranged in*

two rows), with two of said at least two ground terminals being located at the outermost ends of one of said plurality of rows (*FIG. 6: The upper row that includes terminals 1, 3, 5, 7, and 9*).

Referring to claims 4, 10: wherein said plurality of terminals include a clock signal terminal, said clock signal terminal being located between two of said at least two ground terminals (*FIG. 6 and column 7, lines 32-38: The SHIFT terminal*).

Referring to claim 5: wherein said plurality of terminals include a power supply terminal, two of said at least two ground terminals being located at the outermost ends of a row different than the row that contains said power supply terminal (*FIG. 6*).

2. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murray et al. (US 5610635) in view of Nagata et al. (US 5838549), as applied to claims 1 and 3-5, and further in view of Ito et al. (US 5748179).

Murray et al., as modified, discloses the claimed invention as discussed above but is silent wherein said plurality of terminals are arranged at intervals of approximately 1 mm in the direction of formation of said rows.

Ito et al. discloses a circuit board having a plurality of terminals are arranged at intervals of approximately 1 mm in the direction of formation of said rows (*column 7, lines 51-55*).

Therefore, it would have been obvious for one having ordinary skill in the art at the time invention was made to modify the plurality of terminals disclosed by Murray et al., as modified, to locate the terminal at interval of approximately 1mm from each other as disclosed by Ito et al. The motivation for doing so would have been to reduce the noise interference due to the close position of the electrical terminals as well known in the art.

Response to Arguments

Applicant's arguments with respect to claims 1 and 8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAM S. NGUYEN whose telephone number is (571)272-2151. The examiner can normally be reached on 7:00AM - 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, STEPHEN D. MEIER can be reached on (571)272-2149. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LN
July 5, 2005

HAI PHAM
PRIMARY EXAMINER